ABSTRACT OF THE DISCLOSURE

1   Disclosed herein is an organization of cache memory for hardware acceleration of the FDTD

2   method. The organization of cache memory for hardware acceleration of the FDTD method

3   provides a substantial speedup to the finite-difference time-domain (FDTD) algorithm when

4   implemented in a piece of digital hardware. The organization of cache memory for hardware

5   acceleration of the FDTD method utilizes a very high bandwidth dual-port on-chip memory in a

6   particular way. By creating many small banks of internal memory and arranging them carefully, all

7   data dependencies can be statically wired. This allows for a many-fold speedup over SRAM-based

8   solutions and removes the burden of data dependence calculation that streaming SDRAM-based

9   solutions must perform.